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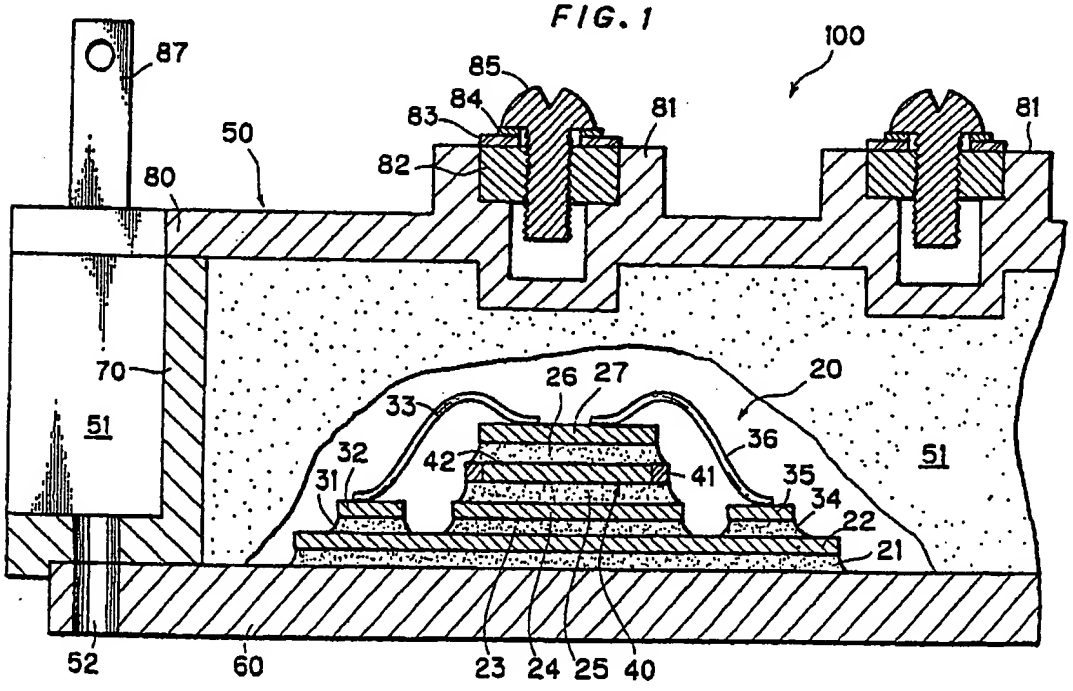
(54) Semiconductor device and soldering method employable in manufacturing the same.

(57) A semiconductor chip (27) is soldered on an electrode plate (24) with a thermal relaxation plate (40) therebetween. The thermal relaxation plate has a frame member (41) made of covar or invar and a plate member (42) made of copper. The plate member is inserted into the window space defined in the frame member and is united with the frame member.

FIG. 1



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SEMICONDUCTOR DEVICE AND SOLDERING METHOD EMPLOYABLE IN MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a soldering method for its manufacture, and particularly to improvement of a thermal stress relaxation member equipped to relax the thermal stress in a semiconductor chip and a method of soldering the semiconductor chip on a prescribed member using the improved thermal stress relaxation member.

Description of the Background Art

As known well in semiconductor device manufacturing technology, there are many cases wherein a semiconductor chip formed with desired active regions is soldered on a prescribed member such as an electrode plate. Fig. 6 shows a partial section showing conventional typical soldered structure of a semiconductor chip 9. As shown in Fig. 6, a heat diffusion plate 1, an insulating base plate 3, an electrode plate 5 and a thermal stress relaxation plate 7 are soldered consecutively by using solder layers 2, 4 and 6. The semiconductor chip 9 is soldered on the thermal stress relaxation plate 7 through a solder layer 8. In case the semiconductor chip 9 is a power transistor, for example, the electrode plate 5 corresponds to a collector electrode plate. In addition, the other electrode plates for the semiconductor chip 9, that is, an emitter electrode plate and a base electrode plate (not shown) are connected to the semiconductor chip 9 through metallic wires 10.

Among these members, the thermal stress relaxation plate 7 is equipped in order to relax thermal stress generating within the semiconductor chip 9 during soldering process. In case the semiconductor chip 9 is made of silicon and the metallic collector plate 5 is made of copper, since coefficient of thermal expansion of the collector metallic plate 5 is around five times as much as that of the semiconductor chip 9, difference between respective shrinking is great when these are cooled from high temperature conditions in soldering. Accordingly, if the thermal stress relaxation plate 7 is not equipped, the thermal stress corresponding to this difference is directly applied to the semiconductor chip 9 to deteriorate electric characters and strength thereof. Furthermore, the thermal stress relaxation plate 7 is effective for relaxing thermal stress due to heat which is generated during electric current flow through the semiconductor chip 9.

Since the thermal stress relaxation plate 7 is provided for these reasons, the thermal stress relaxation plate 7 must be made of material of which coefficient of thermal expansion is comparatively similar to that of silicon. Besides since heat which generates during operation of the semiconductor chip 9 must be quickly transmitted to the heat diffusion plate 1, large thermal conductivity is necessary for the plate 7. Therefore, a molybdenum flat plate is widely used as a conventional thermal stress relaxation plate 7.

However, the molybdenum flat plate is formed by sintering and is very high in the cost, so that the cost of the semiconductor device equipped with the structure in Fig. 6 is also high.

In addition, as thermal conductivity of the molybdenum is not so large, efficiency of transmitting to the heat diffusion plate 1 the heat generating during operation of the semiconductor chip 9 is not so high. In other words, in case the molybdenum flat plate is used as the thermal stress relaxation plate 7, it is difficult to reduce transient thermal resistance thereof. This problem turns out to be especially serious upon a transistor for large electric power in which high speed switching operation is repeated.

In order to cope with such a problem, technology using a copper plate embedded with carbon fibers is disclosed in Japanese Patent Laying-Open Gazettes No. 58-32423 (1983) and No. 57-124459 (1982). In this technology, high thermal conductivity is secured by copper and coefficient of thermal expansion is lowered by carbon fibers.

However, in order to suppress thermal expansion of the copper plate, a lot of carbon fibers must be embedded within the copper plate. On the occasion, local warping generates on the thermal stress relaxation plate in high temperature soldering using hard solder. Actually, in the above-indicated Gazette No. 57-124459, it is described that when soldering is carried out above 700 °C, the warping of the thermal stress relaxation plate suddenly increases.

In addition, since the thermal conductivity and the electric conductivity of carbon fibers are low as compared with those of metal, if large quantity of carbon fibers is embedded, the total thermal conductivity

and the total electric conductivity of the are deteriorated.

SUMMARY OF THE INVENTION

According to the present invention, a semiconductor device comprises (a) a conductive member having electric conductivity, (b) a first solder layer provided on the conductive member, (c) a composite plate member provided on the first solder layer and comprising (c-1) at least one frame member made of a first material and having a window space therein, and (c-2) a plate member made of a second material which is inserted into the window space and is unified with the frame member so that the plate member is substantially in contact with the first solder member through a first opening of the window space, (d) a second solder member provided on the composite plate member so that the composite plate member is substantially in contact with the second solder member through a second opening of the window space, and (e) a semiconductor chip provided on the second solder layer. The first material has a coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of the semiconductor chip, and the second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys.

The present invention also provides a thermal stress relaxation plate employable in a semiconductor device for relaxing a thermal stress in a semiconductor chip, comprising (a) at least one frame member made of a first material and having a window space therein, and (b) a plate member made of a second material which is inserted into the window space and is unified with the frame member so that the plate member has two surfaces which expose at respective window openings of the window space, wherein the first material has coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of the semiconductor chip, and the second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys.

In an aspect of the present invention, provided is a method of soldering a semiconductor chip on a prescribed position, comprising the steps of (a) preparing a composite plate member comprising at least one frame member made of a first material and having a window space therein, and a plate member made of a second material which is inserted into the window space and is unified with the frame member so that the plate member exposes at first and second openings of the window space, wherein the first material has a coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of the semiconductor chip, and the second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys, (b) soldering the composite plate member on the prescribed position while making the first opening face to the prescribed position, and (c) soldering the semiconductor chip on the composite plate member while making the semiconductor chip face to the second opening.

According to the semiconductor device of the present invention, either of copper, aluminum, or their alloys is used as a plate member in the composite plate member, so that thermal conductivity and electric conductivity of the composite plate member is high as a whole. In addition, since a frame member is made of an alloy having coefficient of thermal expansion three times as high as or less than that of a semiconductor chip to suppress thermal expansion of a plate member, a relaxation effect of the whole composite plate member against thermal stress of a semiconductor chip is large. As the composite member of the present invention can be composed without incorporating such materials as sintered molybdenum and carbon fibers, they are low in cost and usable even under high soldering temperature conditions. In addition, according to the soldering method of the present invention, a semiconductor device with the above characteristics can be obtained without complicate process.

Accordingly, an object of the present invention is to provide a low cost semiconductor device equipped with a thermal stress relaxation member which is high in thermal conductivity and electric conductivity and is less in restriction on a soldering temperature.

Another object of the present invention is to provide a method of soldering a semiconductor chip for manufacturing such a semiconductor device.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial sectional view of a semiconductor device according to a preferred embodiment of the

present invention,

Fig. 2 and Fig. 3 are a plane view and an elevation view of the semiconductor device in Fig. 1, respectively,

Fig. 4 and Fig. 5 are perspective views of thermal stress relaxation plates with part taken away, and

Fig. 6 is a partial sectional view showing conventional soldering structure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 and 3 are a plane view and an elevation view showing external appearance of a semiconductor device 100 according to a preferred embodiment of the present invention, respectively. Fig. 1 is an enlarged partial sectional view along line I-I in Fig. 2. The semiconductor device 100 comprises a plurality of power transistor assemblies 20 schematically shown in Fig. 3 and a casing 50 receiving these assemblies 20. The casing 50 has a heat diffusion plate 60 made of copper as a bottom plate on which a resin side member 70 is fixed with an adhesive agent. A resin lid 80 is fixed on the side member 70 so that it covers upper opening of the side member 70.

On the both edges of the casing 50, concaves 51 are formed. As shown in Fig. 1, at the bottom of each concave 51, a fitting hole 52 used for fixing the semiconductor device 100 to a desired position is provided. On the other hand, convexes 81 are provided on three positions of the lid 50. A nut 82 (Fig. 1) is pressed into the convex 81, and a bolt 85 is screwed into the nut 82 through an external electrode plate 83 and a washer 84. External wires such as bus bars are connected to the external electrode plate 83 through combination of the bolt 85 and the nut 82. Though not shown in Fig. 1-3, one edge of each external electrode plate 83 is bent, and electrically connected through the lid 80 to an electrode inside the power transistor assembly 20 in the casing 50.

Fastening terminals 87 are installed on the top of the casing 50, and a control signal for the transistor assembly 20 is applied to the fastening terminals 87, and then transmitted to a control electrode in the assembly 20 through internal wiring not shown. A status in which part is removed is depicted in Fig. 1, but in order to protect from outside atmosphere the transistor assemblies 20 and each internal wire, the transistor assemblies 20 are sealed with resin 51 inside an internal space of the casing 50.

Each of the transistor assemblies 20 is manufactured as follows (refer to Fig. 1) : An insulating base plate 22 made of alumina-ceramics is soldered on the heat diffusion plate 60 through a solder layer 21. A collector electrode plate 24 made of copper is soldered on the center of the upper surface of the insulating base plate 22 through a solder layer 23. On the top surface of this collector electrode plate 24, a thermal stress relaxation plate 40 is soldered through a solder layer 25. The structure of this thermal stress relaxation plate 40 will be described later in detail.

On the thermal stress relaxation plate 40, a semiconductor chip 27 is soldered through a solder layer 26. The semiconductor chip 27 is formed by selectively doping impurities into a silicon substrate and is a power transistor containing junctions between a plurality of active regions.

On the top surface of the insulating base plate 22, an emitter electrode plate 32 made of copper is soldered through a solder layer 31. Likewise, a base electrode plate 35 made of copper is soldered on the plate 22 through a solder layer 34. These emitter electrode plate 32 and base electrode plate 35 are connected to an emitter region and a base region of the semiconductor chip 27 through aluminum wires 33 and 36, respectively. The other ones of the transistor assemblies 20 not shown in Fig. 1 also have the same structure, a plurality of the transistor assemblies 20 being connected each other through wiring and their output being led to the external electrode plates 83.

Fig. 4 is a perspective view of the thermal stress relaxation plate 40 with part taken away. The thermal stress relaxation plate 40 comprises a rectangular frame member 41 and a rectangular plate member 42 inserted into a window space W_1 defined by the frame member 41. The members 41 and 42 are united with each other to form the thermal stress relaxation plate 40. The frame member 41 is made of invar (an alloy consisting of Fe = 63.4%, Ni = 36%, Mn = 0.4% and C = 0.2%), and the plate member 42 is made of copper.

This thermal stress relaxation plate 40 may be obtained by rolling an assembly in which a copper plate is inserted into a rectangular invar frame. Owing to this rolling, a gap between the frame member 41 and the plate member 42 disappears, so that the members 41 and 42 are unified.

The top and bottom surface of the thermal stress relaxation plate 40 are substantially flat, and the plate member 42 is exposed through the upper and lower openings P_1 and P_2 of the window space W_1. In addition, on each surface of the frame member 41 and the plate member 42, nickel plating is applied for attaining tight soldering of the plate 40. Therefore, in case the thermal stress relaxation plate 40 is mounted as shown in Fig. 1, the plate member 42 is substantially in contact with the solder layers 25 and 26.

The frame member 41 may be made of covar (an alloy consisting of Hi = 23 - 30 %, Co = 30 - 17 %, Mn = 0.6 - 0.8 % and Fe = balance) in place of invar. In case the frame member 41 is made of the covar, nickel plating is also applied to the surface. In Table 1, thermal conductivity and coefficient of thermal expansion are shown for invar, covar, copper and silicon, respectively. Besides these values are shown also for molybdenum for comparison with conventional technology.

Table 1

	Thermal conductivity	Coefficient of thermal expansion
	(W / mm $^{\circ}$ C)	(10^{-6} / $^{\circ}$ C)
Invar	0.016	5.5
Covar	0.017	5.1
Copper	0.39	17.1
Silicon	0.16	3.5
Molybdenum	0.13	5.0

As understood from Table 1, the thermal conductivity of copper which is used for the plate member 42 is three times as large as that of molybdenum. Besides though not shown in Table 1, copper is extremely high in electric conductivity. Accordingly, the thermal conductivity and the electric conductivity in an orthogonal-to-plane direction Z direction in Fig. 4) through the plate member 42 become extremely high in the thermal stress relaxation plate 40. Therefore, not only heat transmission during soldering is made favorable, but also transient thermal resistance during an electric current flows through the semiconductor chip becomes less. As a result, the plate 40 can be satisfactorily used for a high speed switching transistor for large power use.

On the other hand, since the plate member 42 is made of the same material, copper, as that of the collector electrode plate 24 and its coefficient of thermal expansion around five times as high as that of silicon, thermal stress due to difference of the coefficient of thermal expansion between the collector electrode plate 24 and the semiconductor chip 27 cannot be relaxed only by the plate member 42. However, as the coefficient of thermal expansion of invar or covar, which is the material of the frame member 41, is approximately the same as silicon, thermal expansion in intra-plane direction (an X-Y direction) of the plate member 41 can be suppressed by the frame member 41. More particularly, the coefficient of thermal expansion in the X- Y plane is around 6.0 x 10^{-6} / $^{\circ}$C as a whole in the thermal stress relaxation plate 40. Though the thermal expansion in the Z direction of the plate member 42 increases owing to the suppression of the thermal expansion in the X-Y plane, overall expansion of the plate member 42 in the Z direction does not result in causing stress within the semiconductor chip 27 and, therefore, this phenomenon causes no practical problems.

That is to say, the thermal stress relaxation plate 42 is formed as a composite plate member consisting of the frame member 41 and the plate member 42, so that the members 41 and 42 meet the first requirement, i.e., improvement of the thermal conductivity and the electric conductivity, and the second requirement, i.e., keeping the coefficient of thermal expansion lower, respectively. In addition, different from the conventional technology in which organic materials such as carbon fibers are embedded within a copper plate, the thermal stress relaxation plate 40 is composed as a combination of metals and alloys. Accordingly, the coupling surface between the members 41 and 42 in the thermal stress relaxation plate 40 is stable and usable at a comparatively high temperature to allow soldering with hard solder. Besides there is also no lowering of the electric conductivity due to embedding great quantity of the carbon fibers.

Fig. 5 is a perspective view of a thermal stress relaxation plate according to another preferred embodiment of the present invention, in which part thereof is taken away. This thermal stress relaxation plate 43 is a composite plate member in which rectangular grid-like frame members 44 and 46 having the same configration each other are mutually arranged in parallel, and a plate material 45 is inserted between them. Also in this example, the frame members 44 and 46 are made of invar or covar, and the plate member 45 is made of copper.

The thermal stress relaxation plate 43 may be obtained from preparing an assembly in which a copper

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flat plate is sandwiched between one pair of grid-like invar frames or covar frames and rolling this assembly. Each surface of the frame members 44 and 46 and the plate member 45 is nickel-plated as that of the thermal stress relaxation plate 40.

The plate member 45 has a center portion 45a extending in an X-Y plane direction and matrix arrangements of convexes 45b and 45c projecting up-and -downward from the portion 45a, respectively. In the matrix arrangement of window spaces W_2 defined by the frame members 44 and 46, the convexes 45b exposes through the bottom openings Q_1 and the other convexes 45c expose through the bottom openings Q_2. Accordingly, in each of the window spaces W_2, the plate member 45 extends from the bottom opening Q_1 of the window space W_2 to the top opening Q_2, so that thermal conductivity and electric conductivity in the Z direction are secured by the plate member 45 as the case of the thermal stress relaxation plate 40. In addition, when the thermal stress relaxation plate 43 is used in place of the thermal stress relaxation plate 40 in Fig. 1, the plate member 45 substantially contacts with the solder layers 25 and 26.

Thermal expansion in the X-Y plane direction within the thermal stress relaxation plate 43 is limited substantially by the coefficient of thermal expansion of the flame members 44 and 46. Therefore this thermal stress relaxation plate 43 also possesses favorable properties of thermal conductivity, electric conductivity and thermal expansion.

Since invar, covar and copper are considerably lower in price compared to that of molybdenum, the semiconductor device 100 manaufactured using the thermal stress relaxation plate 40 or 43 is also lower in cost.

In the following, materials usable for a thermal stress relaxation plate in the present invention are furthermore discussed. To begin with, as regards to characteristics required for the frame members 41, 44 and 46, it is necessary for their coefficients of thermal expansion to be comparatively near to that of the semiconductor chip 27. What a range of coefficient of thermal expansion is allowed depends on soldering conditions, but if their coefficient of thermal expansion is equal to or less than three times the coefficient of thermal expansion of the semiconductor chip 27, a practical thermal stress relaxation effect can be obtained. In case the semiconductor chip 27 is made of silicon, it is understood from Table 1 that an alloy with the coefficient of thermal expansion equal to or less than around 10.5×10^{-6} / °C, which is three times 3.5×10^{-6}, may be used as the frame member capable of suppressing inherent thermal expansion of copper. Invar and covar used in the preferred embodiments meet the requirement, as seen from Table 1. Other alloys of iron satisfying the requirement may be employed as the materials of the frame members 41, 44 and 46.

On the other hand, high thermal conductivity and electric conductivity is required for the plate member 42 and 45. Accordingly, a material selected among copper, copper alloys, aluminum and aluminum alloys is employable for plate members 42 and 45. Thermal conductivity of aluminum is 0.24 W/mm °C, being around twice that of molybdenum. On the other hand, as an example of a usable copper alloy, there is copper containing 0.15 - 0.20 % tin, its thermal conductivity being 0.35 W/mm °C. Further, as an example of an aluminum alloy usable for the plate members 42 and 45, there is aluminum containing 1-2 % silicon.

The present invention is also appliable for soldering a semiconductor chip made of a semiconductor material other than silicon such as GaAs, and for all semiconductor devices in which semiconductor chips are soldered to a designated position or member.

As described above, according to the present invention, a composite plate member composed of a plate member having high in thermal conductivity and high electric conductivity and a frame member with coefficient of thermal expansion comparatively close to a semiconductor chip is used as a thermal stress relaxation member, and these member can be made without using costly materials. Accordingly, a semiconductor device comprising a thermal stress relaxation member having high thermal conductivity and high electric conductivity can be obtained at lower cost.

In addition, as organic fibers such as carbon fibers are not used, the thermal stress relaxation member according to the present invention can be used in high temperature soldering and the allowable limit of the soldering temperature is improved.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation. The spirit and scope of the present invention should be limited only by the terms of the appended claims.

Claims

1. A semiconductor device comprising;
(a) a conductive member having electric conductivity;

(b) a first solder layer provided on said conductive member;
(c) a composite plate member provided on said first solder layer and comprising;
(c-1) at least one frame member mae of a first material and having a window space therein; and
(c-2) a plate member mae of a second material which is inserted into said window space and is united with said frame member so that said plate member is substantially in contact with said first solder member through a first opening of said window space;
(d) a second solder member provided on said composite plate member so that said composite plate member is substantially in contact with said second solder member through a second opening of said window space; and
(e) a semiconductor chip provided on said second solder layer;
wherein said first material has a coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of said semiconductor chip, and said second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys.

2. The semiconductor device of claim 1, wherein;
said frame member has only one window space; and
said plate member is a flat plate member inserted into said only one window space.

3. The semiconductor device of claim 1, wherein;
said at least one frame member comprises;
(c-1a) a first frame member having a plurality of first windows therein;
(c-1b) a second frame member having a plurality of second windows therein and arranged in parallel with said first frame member across a gap so that said plurality of first windows are aligned with said plurality of second windows, respectively; and
said plate member comprises;
(c-2a) a center portion inserted into said gap;
(c-2b) a plurality of first convex portions projecting from said center portion into said plurality of first windows; and
(c-2c) a plurality of second convex portions projecting from said center portion into said plurality of second windows.

4. A semiconductor device of claim 3. wherein;
said plurality of first windows are arranged in a matrix array; and
said plurality of second windows are also arranged in a matrix array.

5. The semiconductor device of claim 1, wherein;
said first material is selected from the group consisting of invar and covar.

6. The semiconductor device of claim 5, wherein;
nickel plating is applied to respective surfaces of said composite plate member facing to said first and second solder layers.

7. The semiconductor device of claim 1, wherein;
said conductive member is an electrode plate for said semiconductor chip.

8. The semiconductor device of claim 7, further comprising;
(f) a heat diffusion plate on which said conductive member is soldered through an insulating plate.

9. The semiconductor device of claim 8, wherein;
said composite plate member serves as a thermal stress relaxation plate for relaxing a thermal stress in said semiconductor chip.

10. A thermal stress relaxation plate employable in a semiconductor device for relaxing a thermal stress in a semiconductor chip, comprising
(a) at least one frame member made of a first material and having a window space therein; and
(b) a plate member made of a second material which is inserted into said window space and is unitied with said frame member so that said plate member has two surfaces which expose at respective window openings of said window space;
wherein said first material has coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of said semiconductor chip, and said second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys.

11. The thermal stress relaxation plate of claim 10, wherein;
said frame member has only one window space; and
said plate member is a flat plate member inserted into said only one window space.

12. The thermal stress relaxation plate of claim 10, wherein;
said at least one frame member comprises;
(a-1) a first frame member having a plurality of first windows therein;

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(a-2) a second frame member having a plurality of second windows therein and arranged in parallel with said first frame member across a gap so that said plurality of first windows are aligned with said plurality of second windows, respectively; and

said plate member comprises;

(b-1) a center portion inserted into said gap;

(b-2) a plurality of first convex portions projecting from said center portion into said plurality of first windows; and

(b-3) a plurality of second convex portions projecting from said center portion into said plurality of second windows.

13. The thermal stress relaxation plate of claim 12, wherein;

said first material is selected from the group consisting of invar and covar.

14. The thermal stress relaxation plate of claim 13, wherein;

nickel plating is applied to respective surfaces of said frame member and said plate member.

15. A method of soldering a semiconductor chip on a prescribed position, comprising the steps of;

(a) preparing a composite plate member comprising;

at least one frame member made of a first material and having a window space therein; and a plate member made of a second material which is inserted into said window space and is united with said frame member so that said plate member exposes at first and second openings of said window space; wherein said first material has a coefficient of thermal expansion equal to or less than three times a coefficient of thermal expansion of said semiconductor chip, and said second material is selected from the group consisting of copper, copper alloys, aluminum and aluminum alloys;

(b) soldering said composite plate member on said prescribed position while making said first opening face to said prescribed position; and

(c) soldering said semiconductor chip on said composite plate member while making said semiconductor chip face to said second opening.

16. The method of claim 15, wherein;

the step (a) includes the steps of;

(a-1) preparing a frame made of said first material and a plate made of said second material;

(a-2) inserting said plate into a window of said frame; and

(a-3) rolling said plate together with said frame to obtain said composite plate member.

17. The method of claim 16, wherein;

said first material is selected from the group consisting of invar and covar.

18. The semiconductor device of claim 17, wherein;

nickel plating is applied to respective surfaces of said composite plate member.

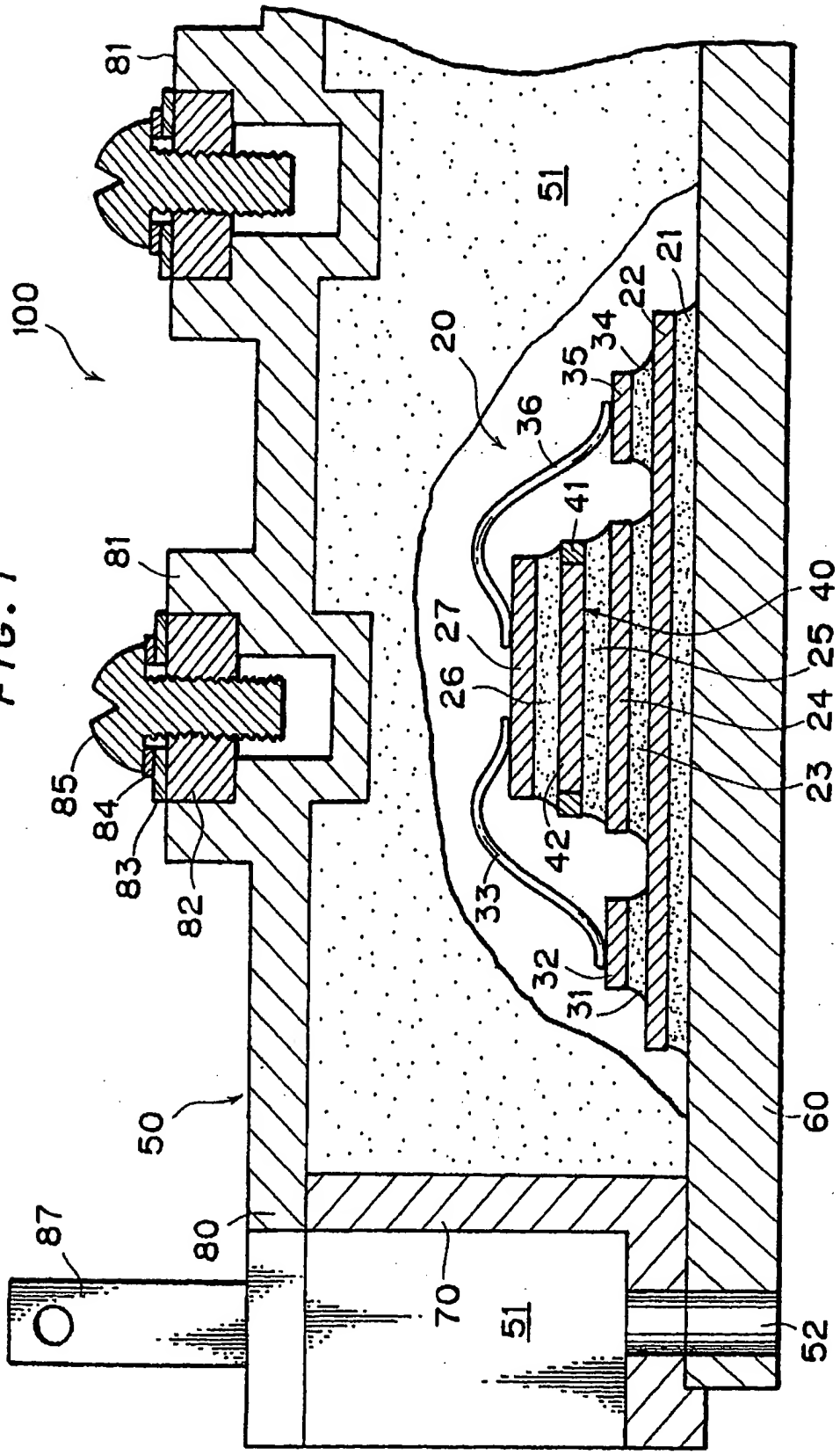
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FIG. 1

FIG. 2

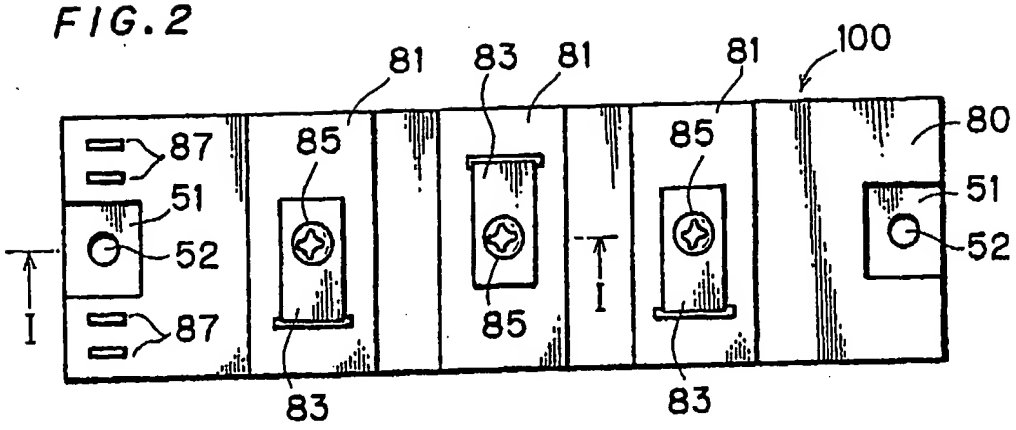


FIG. 3

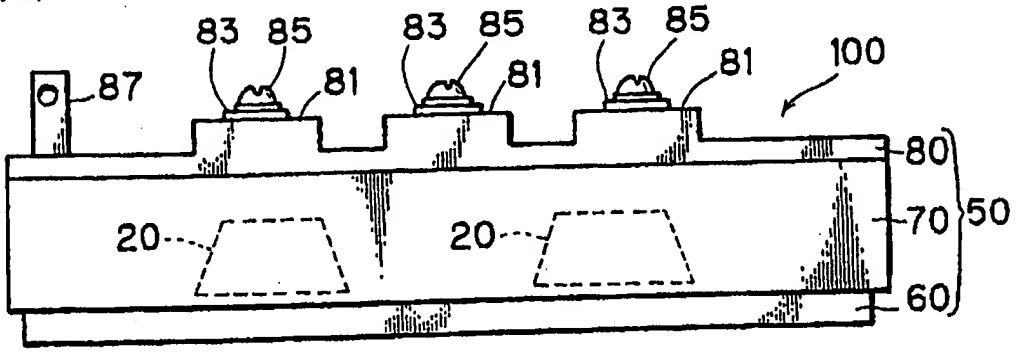


FIG. 6

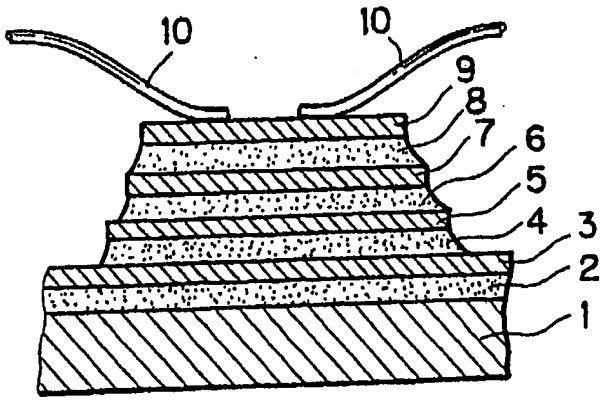


FIG. 4

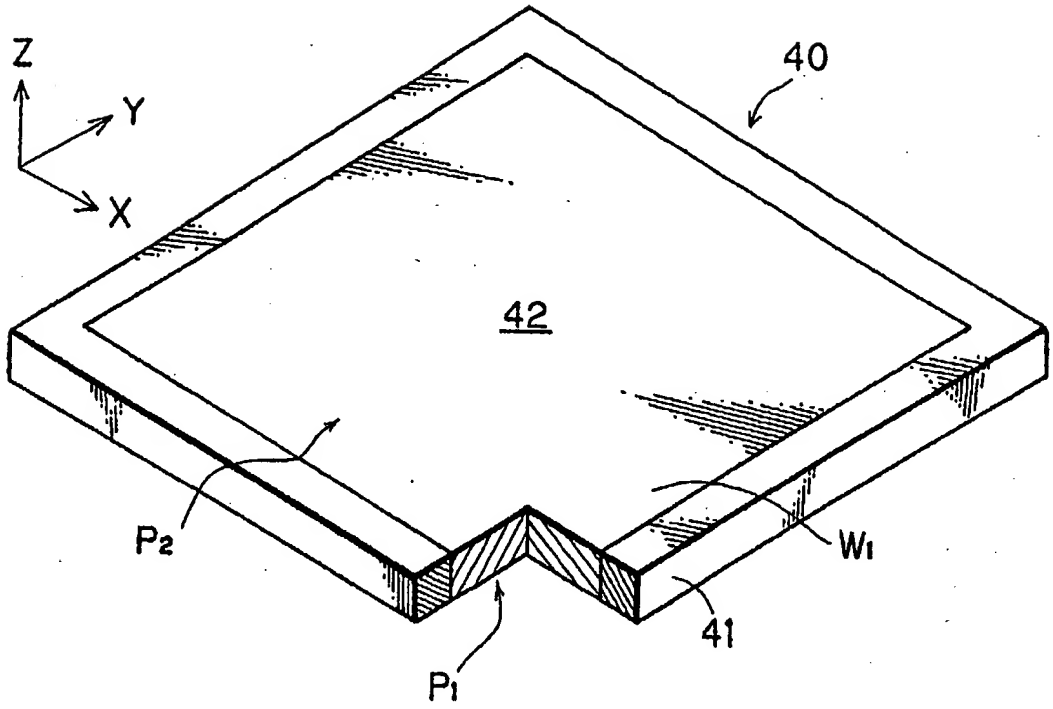
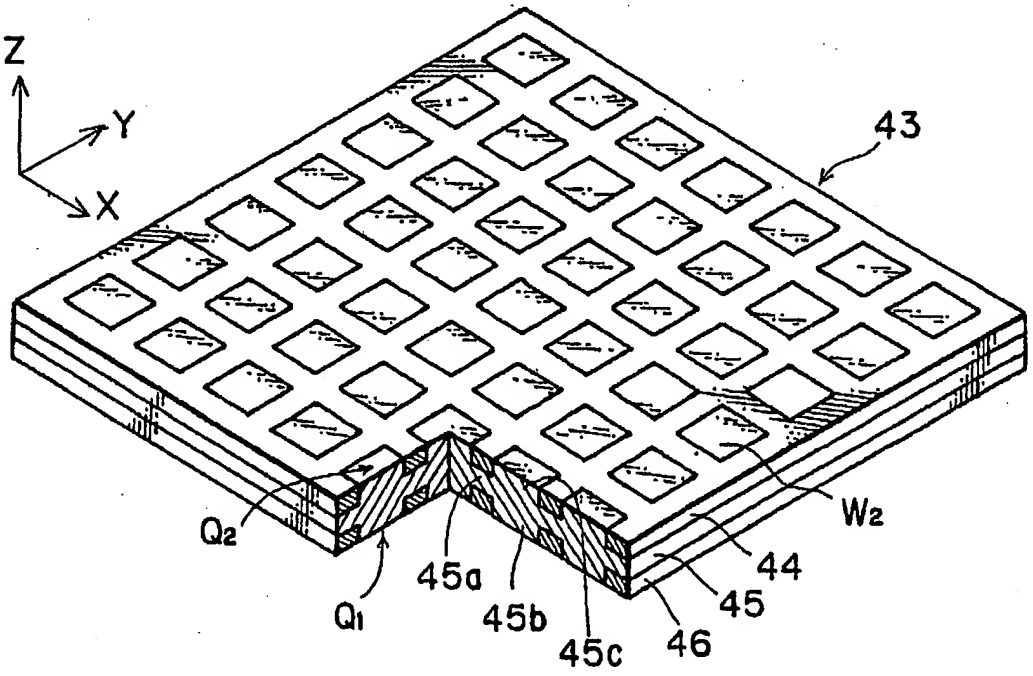


FIG. 5



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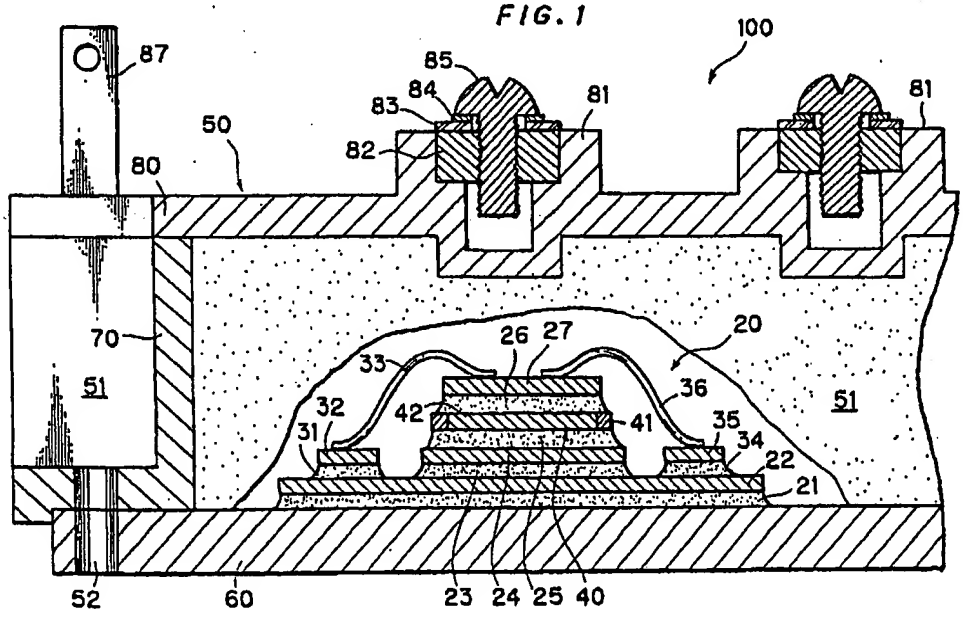
(54) **Semiconductor device and soldering method employable in manufacturing the same.**

(57) A semiconductor chip (27) is soldered on an electrode plate (24) with a thermal relaxation plate (40) therebetween. The thermal relaxation plate has a frame member (41) made of covar or invar and a plate member (42) made of copper. The plate member is inserted into the window space defined in the frame member and is united with the frame member.

FIG. 1



EP 0 424 858 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 12 0253

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	DE-A-3 144 759 (GENERAL ELECTRIC CO.) * the whole document *	1,5-10, 14-18	H01L23/492 H01L23/373 H01L25/07
A		3,12,13	H01L21/60
X	GB-A-2 048 567 (N. HASCOE) * the whole document *	1,3-5, 10,12,13	
D,A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 111 (E-175)14 May 1983 & JP-A-58 032 423 (HITACHI SEISAKUSHO KK) 25 February 1983 * abstract *	1-9,15	
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 218 (E-200)28 September 1983 & JP-A-58 111 353 (HITACHI SEISAKUSHO KK) 2 July 1983 * abstract *	1-9,15	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 MARCH 1992	ZEISLER P.W.

CATEGORY OF CITED DOCUMENTS

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